

WHAT IS CLAIMED IS:

1. A heterojunction type compound semiconductor field effect transistor comprising:

5 a channel layer provided on a compound semiconductor substrate and composed of intrinsic GaAs or InGaAs;

a first electron supply layer provided on the channel layer and composed of AlGaAs doped with n type impurities;

10 an electric field strength reducing layer provided on the first electron supply layer and composed of intrinsic InGaP;

a first contact layer provided on the electric field strength reducing layer and composed of GaAs or
15 InGaAs doped with n type impurities;

a recess stopper layer provided on the first contact layer and composed of intrinsic InGaP;

a second contact layer provided on the recess stopper layer and composed of GaAs doped with n type
20 impurities of a concentration higher than that of the first contact layer;

a wide recess opening formed to penetrate the second contact layer so as to expose a surface of the recess stopper layer;

25 a narrow recess opening formed in the wide recess opening to penetrate the recess stopper layer, the first contact layer, and the electric field strength

reducing layer so as to expose a surface of the first electron supply layer;

5 a gate electrode provided on the surface of the first electron supply layer exposed from a bottom of the narrow recess opening; and

a source electrode and a drain electrode provided on the second contact layer outside the wide recess opening so that the wide recess opening is sandwiched between the source electrode and the drain electrode.

10 2. The heterojunction type compound semiconductor field effect transistor according to claim 1, wherein each of the electric field strength reducing layer and the recess stopper layer is thinner than the first contact layer.

15 3. The heterojunction type compound semiconductor field effect transistor according to claim 1, wherein the compound semiconductor substrate includes a semi-insulating GaAs substrate, a buffer layer provided on the semi-insulating GaAs substrate and having a
20 superlattice structure, and a second electron supply layer provided on the buffer layer and under the channel layer and composed of AlGaAs doped with n type impurities.

25 4. A heterojunction type compound semiconductor field effect transistor comprising:

a channel layer provided on a compound semiconductor substrate and composed of intrinsic GaAs or

InGaAs;

a first electron supply layer provided on the channel layer and composed of AlGaAs doped with n type impurities;

5 an electric field strength reducing layer provided on the first electron supply layer and composed of intrinsic InGaP;

a first contact layer provided on the electric field strength reducing layer and composed of GaAs or
10 InGaAs doped with n type impurities;

a recess stopper layer provided on the first contact layer and composed of intrinsic InGaP;

a second contact layer provided on the recess stopper layer and composed of GaAs doped with n type
15 impurities of a concentration higher than that of the first contact layer;

a wide recess opening formed to penetrate the second contact layer and the recess stopper layer so as to expose a surface of the first contact layer;

20 a narrow recess opening formed in the wide recess opening to penetrate the first contact layer and the electric field strength reducing layer so as to expose a surface of the first electron supply layer;

a gate electrode provided on the surface of the
25 first electron supply layer exposed from a bottom of the narrow recess opening; and

a source electrode and a drain electrode provided

on the second contact layer outside the wide recess opening so that the wide recess opening is sandwiched between the source electrode and the drain electrode.

5 5. The heterojunction type compound semiconductor field effect transistor according to claim 4, wherein each of the electric field strength reducing layer and the recess stopper layer is thinner than the first contact layer.

10 6. The heterojunction type compound semiconductor field effect transistor according to claim 4, wherein the compound semiconductor substrate includes a semi-insulating GaAs substrate, a buffer layer provided on the semi-insulating GaAs substrate and having a superlattice structure, and a second electron supply
15 layer provided on the buffer layer and under the channel layer and composed of AlGaAs doped with n type impurities.

7. A heterojunction type compound semiconductor field effect transistor comprising:

20 a channel layer provided on a compound semiconductor substrate and composed of intrinsic GaAs or InGaAs;

25 a first electron supply layer provided on the channel layer and composed of AlGaAs doped with n type impurities;

an electric field strength reducing layer provided on the first electron supply layer and composed of

intrinsic InGaP;

a first contact layer provided on the electric field strength reducing layer and composed of GaAs or InGaAs doped with n type impurities;

5 a recess stopper layer provided on the first contact layer and composed of intrinsic InGaP;

a second contact layer provided on the recess stopper layer and composed of GaAs doped with n type impurities of a concentration higher than that of the first contact layer;

10 a wide recess opening formed to penetrate the second contact layer so as to expose a surface of the recess stopper layer;

a narrow recess opening formed in the wide recess opening to penetrate the recess stopper layer and the first contact layer so as to expose a surface of the electric field strength reducing layer;

15 a gate electrode provided on the surface of the electric field strength reducing layer exposed from a bottom of the narrow recess opening; and

20 a source electrode and a drain electrode provided on the second contact layer outside the wide recess opening so that the wide recess opening is sandwiched between the source electrode and the drain electrode.

25 8. The heterojunction type compound semiconductor field effect transistor according to claim 7, wherein each of the electric field strength reducing layer and

the recess stopper layer is thinner than the first contact layer.

9. The heterojunction type compound semiconductor field effect transistor according to claim 7, wherein
5 the compound semiconductor substrate includes a semi-insulating GaAs substrate, a buffer layer provided on the semi-insulating GaAs substrate and having a superlattice structure, and a second electron supply layer provided on the buffer layer and under the
10 channel layer and composed of AlGaAs doped with n type impurities.

10. A heterojunction type compound semiconductor field effect transistor comprising:

a channel layer provided on a compound
15 semiconductor substrate and composed of intrinsic GaAs or InGaAs;

a first electron supply layer provided on the channel layer and composed of AlGaAs doped with n type impurities;

20 an electric field strength reducing layer provided on the first electron supply layer and composed of intrinsic InGaP;

a first contact layer provided on the electric field strength reducing layer and composed of GaAs or
25 InGaAs doped with n type impurities;

a recess stopper layer provided on the first contact layer and composed of intrinsic InGaP;

a second contact layer provided on the recess stopper layer and composed of GaAs doped with n type impurities of a concentration higher than that of the first contact layer;

5 a wide recess opening formed to penetrate the second contact layer and the recess stopper layer so as to expose a surface of the first contact layer;

 a narrow recess opening formed in the wide recess opening to penetrate the first contact layer so as to
10 expose a surface of the electric field strength reducing layer;

 a gate electrode provided on the surface of the electric field strength reducing layer exposed from a bottom of the narrow recess opening; and

15 a source electrode and a drain electrode provided on the second contact layer outside the wide recess opening so that the wide recess opening is sandwiched between the source electrode and the drain electrode.

20 11. The heterojunction type compound semiconductor field effect transistor according to claim 10, wherein each of the electric field strength reducing layer and the recess stopper layer is thinner than the first contact layer.

25 12. The heterojunction type compound semiconductor field effect transistor according to claim 10, wherein the compound semiconductor substrate includes a semi-insulating GaAs substrate, a buffer layer provided

on the semi-insulating GaAs substrate and having
a superlattice structure, and a second electron supply
layer provided on the buffer layer and under the
channel layer and composed of AlGaAs doped with n type
5 impurities.

13. A manufacturing method for a heterojunction
type compound semiconductor field effect transistor,
the method comprising:

forming a channel layer composed of intrinsic GaAs
10 or InGaAs on a compound semiconductor substrate;

forming a first electron supply layer composed of
AlGaAs on the channel layer;

forming an electric field strength reducing layer
composed of intrinsic InGaP on the electron supply
15 layer;

forming a first contact layer composed of GaAs or
InGaAs doped with n type impurities, on the electric
field strength reducing layer;

forming a recess stopper layer composed of
20 intrinsic InGaP, on the first contact layer;

forming, on the recess stopper layer, a second
contact layer composed of GaAs doped with n type
impurities of a concentration higher than that of the
first contact layer;

25 wet-etching the second contact layer to form
a wide recess opening penetrating the second contact
layer using the recess stopper layer as a stopper;

forming a source electrode and a drain electrode on the second contact layer outside the wide recess opening so that the wide recess opening is sandwiched between the source electrode and the drain electrode;

5 wet-etching the first contact layer in the wide recess opening using the electric field strength reducing layer as a stopper;

 wet-etching the electric field strength reducing layer in the wide recess opening to form a narrow
10 recess opening penetrating the recess stopper layer, the first contact layer, and the electric field strength reducing layer using the first electron supply layer as a stopper; and

 forming a gate electrode on a surface of the first
15 electron supply layer exposed from a bottom of the narrow recess opening.

14. The manufacturing method for a heterojunction type compound semiconductor field effect transistor according to claim 13, wherein the compound semiconductor substrate includes a semi-insulating GaAs
20 substrate, a buffer layer deposited and formed on the semi-insulating GaAs substrate and having a superlattice structure, and a second electron supply layer deposited and formed on the buffer layer and
25 under the channel layer and composed of AlGaAs doped with n type impurities.

15. A manufacturing method for a heterojunction

type compound semiconductor field effect transistor,
the method comprising:

forming a channel layer composed of intrinsic GaAs
or InGaAs on a compound semiconductor substrate;

5 forming a first electron supply layer composed of
AlGaAs on the channel layer;

forming an electric field strength reducing layer
composed of intrinsic InGaP on the electron supply
layer;

10 forming a first contact layer composed of GaAs or
InGaAs doped with n type impurities, on the electric
field strength reducing layer;

forming a recess stopper layer composed of
intrinsic InGaP, on the first contact layer;

15 forming, on the recess stopper layer, a second
contact layer composed of GaAs doped with n type
impurities of a concentration higher than that of the
first contact layer;

20 wet-etching the second contact layer using the
recess stopper layer as a stopper;

wet-etching the recess stopper layer to form
a wide recess opening penetrating the second contact
layer and the recess stopper layer using the first
contact layer as a stopper;

25 forming a source electrode and a drain electrode
on the second contact layer outside the wide recess
opening so that the wide recess opening is sandwiched

between the source electrode and the drain electrode;
wet-etching the first contact layer in the wide
recess opening using the electric field strength
reducing layer as a stopper;

5 wet-etching the electric field strength reducing
layer in the wide recess opening to form a narrow
recess opening penetrating the first contact layer
and the electric field strength reducing layer using
the first electron supply layer as a stopper; and
10 forming a gate electrode on a surface of the
electron supply layer exposed from a bottom of the
narrow recess opening.

16. The manufacturing method for a heterojunction
type compound semiconductor field effect transistor
15 according to claim 15, wherein the compound semicon-
ductor substrate includes a semi-insulating GaAs
substrate, a buffer layer deposited and formed on
the semi-insulating GaAs substrate and having a
superlattice structure, and a second electron supply
20 layer deposited and formed on the buffer layer and
under the channel layer and composed of AlGaAs doped
with n type impurities.

17. A manufacturing method for a heterojunction
type compound semiconductor field effect transistor,
25 the method comprising:

forming a channel layer composed of intrinsic GaAs
or InGaAs on a compound semiconductor substrate;

forming a electron supply layer composed of AlGaAs
on the channel layer;

forming an electric field strength reducing layer
composed of intrinsic InGaP on the first electron
5 supply layer;

forming a first contact layer composed of GaAs or
InGaAs doped with n type impurities, on the electric
field strength reducing layer;

forming a recess stopper layer composed of
10 intrinsic InGaP, on the first contact layer;

forming, on the recess stopper layer, a second
contact layer composed of GaAs doped with n type
impurities of a concentration higher than that of the
first contact layer;

15 wet-etching the second contact layer to form
a wide recess opening penetrating the second contact
layer using the recess stopper layer as a stopper;

forming a source electrode and a drain electrode
on the second contact layer outside the wide recess
20 opening so that the wide recess opening is sandwiched
between the source electrode and the drain electrode;

wet-etching the recess stopper layer in the wide
recess opening using the first contact layer as a
stopper;

25 wet-etching the first contact layer in the wide
recess opening to form a narrow recess opening
penetrating the recess stopper layer and the first

contact layer using the electric field strength
reducing layer as a stopper; and

forming a gate electrode on a surface of the
electric field strength reducing layer exposed from
5 a bottom of the narrow recess opening.

18. The manufacturing method for a heterojunction
type compound semiconductor field effect transistor
according to claim 17, wherein the compound semicon-
ductor substrate includes a semi-insulating GaAs
10 substrate, a buffer layer deposited and formed on
the semi-insulating GaAs substrate and having a
superlattice structure, and a second electron supply
layer deposited and formed on the buffer layer and
under the channel layer and composed of AlGaAs doped
15 with n type impurities.

19. A manufacturing method for a heterojunction
type compound semiconductor field effect transistor,
the method comprising:

forming a channel layer composed of intrinsic GaAs
20 or InGaAs on a compound semiconductor substrate;

forming a first electron supply layer composed of
AlGaAs on the channel layer;

forming an electric field strength reducing layer
composed of intrinsic InGaP on the electron supply
25 layer;

forming a first contact layer composed of GaAs or
InGaAs doped with n type impurities, on the electric

field strength reducing layer;

forming a recess stopper layer composed of
intrinsic InGaP, on the first contact layer;

forming, on the recess stopper layer, a second
5 contact layer composed of GaAs doped with n type
impurities of a concentration higher than that of the
first contact layer;

wet-etching the second contact layer using the
recess stopper layer as a stopper;

10 wet-etching the recess stopper layer to form
a wide recess opening penetrating the second contact
layer and the recess stopper layer using the first
contact layer as a stopper;

forming a source electrode and a drain electrode
15 on the second contact layer outside the wide recess
opening so that the wide recess opening is sandwiched
between the source electrode and the drain electrode;

wet-etching the first contact layer in the wide
recess opening to form a narrow recess opening
20 penetrating the first contact layer using the electric
field strength reducing layer as a stopper; and

forming a gate electrode on a surface of the
electric field strength reducing layer exposed from
a bottom of the narrow recess opening.

25 20. The manufacturing method for a heterojunction
type compound semiconductor field effect transistor
according to claim 19, wherein the compound

semiconductor substrate includes a semi-insulating GaAs substrate, a buffer layer deposited and formed on the semi-insulating GaAs substrate and having a superlattice structure, and a second electron supply
5 layer deposited and formed on the buffer layer and under the channel layer and composed of AlGaAs doped with n type impurities.